REMARKS

Applicant has carefully considered the Office Action mailed November 10, 2003. Applicant wishes to express his appreciation to the Examiner for the interview conducted by the undersigned, Applicant's attorney, on Feb. 25, 2004.

The present response is intended to implement the conclusions of the interview, and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application are respectfully requested.

The specification has been amended by correction of typographical errors, etc.

The specification has also been amended to remove the Examiner's objection under Sec. 112 to the use of the term "magic number". The relevant paragraphs have been rewritten for improved clarity, without introducing any new matter.

Independent claim 1 and dependent claims 4, 10-15 and 17-19 have been amended. Claims 2-3, and 5-9 have been deleted. Therefore, claims 1, 4 and 10-19 remain in the case.

It is a principal object of the present invention to more efficiently move data from one CPU to another over a bus such as a PCI bus, using enhanced queue management techniques. The PCI bus is capable of performing write operations significantly faster than read operations, and the invention executes an across-a-computer bus read operation, by substituting for this operation - a plurality of write operations across the PCI bus, and read operations from a local memory.

Claim 1 has been amended to incorporate the recitation of now-deleted subclaims 2-3, and 5-8, so that claim 1 now specifically defines the registers used to implement the write operations across the PCI bus, and the local read operation from the memory of the receiving CPU.

These amendments to claim 1 overcome the Examiner's Sec. 112 rejections, and follow the Examiner's suggestions as indicated in paragraphs 10-11.

The specification has been amended to overcome the Examiner's rejection as indicated in para. 12. It is now clarified that the message separators are of two types, and the specification has been amended to indicate these. Specifically, the text at page 9 now defines a "header-type separator" and "stopper-type separator" (or stopper), the former designating the beginning of a message, the latter the end of a message. This clarification better explains the function of the stopper and the respective "magic number", which is a known queue management technique, used in each of the separators. As indicated in the specification at page 9, line 11, the "magic number" is a predetermined number "which is used by the system to verify correctness of the queue management".

The remaining Sec. 112 rejections as indicated in paras. 14-22 are deemed overcome in light of the claim amendments which further define the system and the components which execute the tasks. During the interview, these claim amendments were reviewed briefly, and were considered acceptable.

The Examiner has rejected the claims under Secs. 102(a) and (e) as being anticipated by Daniel et. al. (USP 6,115,761).

Daniel et al. discloses an elaborate credits system for managing the operation of a FIFO memory which is used to transfer data between two electronic devices or modules. Because a FIFO access routine across a bus may cause a significant system performance bottleneck, Daniel et al. discloses a dual descriptor FIFO arrangement, one per processor, using a pointer. Daniel et al. describes an elaborate credits system so that each processor only has to access its own on-board descriptor, without accessing the bus, to determine if the FIFO is available.

However, Daniel et al. lacks a total read and total write register, as used in the present invention, which simplifies the determination of whether there is sufficient space for a write operation. The queue management technique of the present invention is thus an entirely different approach from Daniel.

Therefore, independent claim 1 is not anticipated under Sec. 102(a) or (e).

As stated in the decision in In Re Marshall, 198 USPQ 344 (1978), "To constitute an anticipation, all material elements recited in a claim must be found in one unit of prior art…". Since the Daniel et al. reference neither 1) identically describes the invention, nor 2) enables one skilled in the art to practice it, Applicant deems the 102(a) and (e) rejection improper, and respectfully requests that it be withdrawn.

The Examiner has rejected the claims under Sec. 103(a) as being unpatentable over Daniel et al., and alternatively, over Daniel et al. in view of Young (USP 6,006,292).

As pointed out above, there is no well-established basis for the Examiner's position that Daniel et al. supports a 102(a) or (e) rejection, since there is no total read and total write register, as in the present invention. However, the Examiner concludes that these types of registers are well known, and that it would have been obvious to include them in the receiving memory to monitor the status of the queue.

To support this conclusion, the Examiner introduces Young, which contains disclosure of a "removed TCB counter 132" (= total read register) and a "queued TCB counter 131" (= total write register).

By review of Fig. 1 of Young, it can be seen that the system has a single removed TCB counter 132, and two queued TCB counters 131, meaning that in terms of the present invention, there is <u>one</u> total read register, and <u>two</u> total write registers. Therefore, the combination of Daniel and Young does not teach a receiving CPU comprising a first total read register, and a

transmitting CPU comprising a second total read register and a total write register, as required by independent claim 1. Thus, as amended, independent claim 1 is not made obvious based on the combination of Daniel and Young, since the combination teaches an architecture different from that recited in independent claim 1.

In addition, from Fig. 1 of Young, it is seen that the Host system contains the circular queue 112, while the sequencer 125 is located in the Host adapter, on the other side of the bus. As stated at col. 3, line 2... "Sequencer 125 uses head pointer 156 to determine the location of the next TCB pointer to transfer". This is essentially a read operation, and since the sequencer operates across the bus from the queue 112, the operation of reading from the queue across the bus indicates clearly that Young does not suggest the present invention, which avoids a direct read operation across the bus.

It is the Applicant's position that the combination of the Daniel et al. and Young references to form the basis of the Sec. 103(a) rejection is improper, and Applicant respectfully requests that it be withdrawn.

Therefore, claim 1 is deemed to be patentable, and dependent claims are deemed to be patentable as being based thereon.

In citing the references under Sec. 103(a), the question is raised whether the references would suggest the invention, as stated in the decision of In Re Lintner (172 USPQ 560, 562, CCPA 1972);

> "In determining the propriety of the Patent Office case for obviousness in the first instance, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the references before him to make the proposed substitution, combination or other modification."

Similarly, In Re Regel (188 USPQ 136, CCPA 1975) decided that the question raised under Sec. 103 is whether the prior art

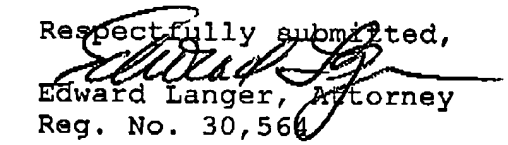
taken as a whole would suggest the claimed invention to one of ordinary skill in the art. Accordingly, even if all the elements of a claim are disclosed in various prior art references, the claimed invention taken as a whole cannot be said to be obvious without some reason given in the prior art why one of ordinary skill would have been prompted to combine the teachings of the references to arrive at the claimed invention.

Simply put, and as stated in In Re Clinton (188 USPQ 365 CCPA 1976), "do the references themselves... suggest doing what appellants have done", such that there is a requirement that the prior art must have made any proposed modification or changes in the prior art obvious to do, rather than obvious to try.

It is respectfully put forward by the Applicant that there is no reason to consider the prior art references, to Daniel et al. and Young, either individually or in combination, as rendering the invention obvious, since neither of them discloses the enhanced queue management techniques disclosed by Applicant. Specifically, the combination thereof does not enable a PCI bus to perform write operations in lieu of read operations, so as to execute an across-a-computer bus read operation, by substituting for this operation - a plurality of write operations across the PCI bus, and read operations from a local memory.

In view of the foregoing remarks, it is believed that the objections have been overcome as suggested by the Examiner, and reconsideration and allowance of the remaining claims at an early date is respectfully requested.

Respectfully submitted,



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